

2019 Batch.

DHABALESWAR INSTITUTE OF POLYTECHNIC LESSON PLAN

Discipline .	Semester - <u>V - 2</u>	Name of the Teaching Faculty - <u>Girija Sanker Pradhan</u>
Subject <u>VLSI & Embedded System</u>	No. of days per Week Class Alloted - <u>4 (Four)</u>	Semester from Dt. <u>4/10/2021</u> To Dt. <u>7/01/2022</u> No. of Weeks: <u>14 (fourteen)</u>
Week	Class Day	Theory / Practical Topics
<u>Oct 1st week 2021</u>	<u>1st Day</u>	<u>Historical perspective</u>
	<u>2nd</u>	<u>Classification of CMOS digital circuits</u>
	<u>3rd</u>	<u>Introduction to MOS Transistors and</u>
	<u>4th</u>	<u>Basic operation of MOSFET</u>
	<u>5th</u>	<u>structure and operation of MOSFET</u>
<u>2nd week</u>	<u>1st</u>	<u>(n-mos enhancement type) & CMOS</u>
<u>3rd</u>	<u>2nd</u>	<u>V-I characteristics of MOSFET</u>
	<u>3rd</u>	<u>Working of MOSFET capacitances</u>
	<u>4th</u>	<u>Modelling of MOS Transistors SPICE</u>
	<u>5th</u>	<u>level 1</u>
<u>4th week</u>	<u>1st</u>	<u>SPICE. level 2 and level 3 Model</u>
	<u>2nd</u>	<u>flow circuit design procedures</u>
	<u>3rd</u>	<u>VLSI design flow & Y-chart</u>
	<u>4th</u>	<u>Design hierarchy</u>
	<u>5th</u>	<u>Simplified process for fabrication</u>
<u>5th (November)</u>	<u>1st</u>	<u>Basic steps in fabrication process</u>
	<u>2nd</u>	<u>fabrication process of n-MOS Transistor</u>
	<u>3rd</u>	<u>CMOS n-well fabrication process</u>
	<u>4th</u>	<u>flow</u>
	<u>5th</u>	<u>MOS fabrication process by n-well on</u>
<u>6th</u>	<u>1st</u>	<u>p-substrate</u>
	<u>2nd</u>	<u>CMOS fabrication process by p-well</u>
	<u>3rd</u>	<u>on a n-substrate</u>
	<u>4th</u>	<u>Lay out Design rules.</u>
	<u>5th</u>	<u>Stick diagram of CMOS inverter</u>
<u>7th</u>	<u>1st</u>	<u>Basic CMOS inverters.</u>
	<u>2nd</u>	<u>Working of Resistive load inverter</u>
	<u>3rd</u>	<u>Inverter with n-type MOSFET load</u>
	<u>4th</u>	<u>Enhancement load, Depletion n-mos</u>
	<u>5th</u>	<u>inverter.</u>
<u>8th</u>	<u>1st</u>	<u>CMOS inverter. circuit operation</u>
	<u>2nd</u>	<u>characteristics and interconnect effect</u>
	<u>3rd</u>	<u>Delay time definitions.</u>
	<u>4th</u>	<u>CMOS inverter design with delay</u>
	<u>5th</u>	<u>constraints.</u>
	<u>1st</u>	<u>Two sample mask layout for p-type substrate</u>

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Week	Class Day	Theory / Practical Topics
	<u>2nd</u>	static combinational logic Working of static CMOS logic circuits (Two input NAND gate)
	<u>3rd</u>	CMOS logic circuits (NAND gate)
	<u>4th</u>	CMOS Transmission gates (Pass gate)
	<u>5th</u>	Complex Logic circuits (Basics)
<u>9th</u>	<u>1st</u>	Classification of Logic circuits based on their temporal behaviour.
	<u>2nd</u>	SR Flip Latch circuit
<u>December</u>	<u>3rd</u>	Clocked SR Latch only
	<u>4th</u>	CMOS D Latch
	<u>5th</u>	Basic principles of Dynamic Pass Transistor circuit
<u>10th</u>	<u>1st</u>	Dynamic RAM, SRAM
	<u>2nd</u>	Flash memory
	<u>3rd</u>	Design Language (SPL & HDL)
	<u>4th</u>	EDA tools & VHDL Xilinx
	<u>5th</u>	Concept of FPGA, standard cell based design.
<u>11th</u>	<u>1st</u>	VHDL for design synthesis using CPLD or FPGA
	<u>2nd</u>	Embedded System Overview, list of embedded systems
	<u>3rd</u>	Characteristics and example
	<u>4th</u>	A digital camera
	<u>5th</u>	Embedded System Technologies
<u>12th</u>	<u>1st</u>	Definition, processor Technology
	<u>2nd</u>	IC Technology
	<u>3rd</u>	Design Technology, processor Technology
	<u>4th</u>	General Purpose processors - Software
	<u>5th</u>	Basic Architecture of single purpose processors - Hardware
<u>13th</u>	<u>1st</u>	Application Specific Processors
	<u>2nd</u>	Microcontroller
	<u>3rd</u>	Digital Signal Processors
14th	<u>4th</u>	IC Technology

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