

DHABALESWAR INSTITUTE OF POLYTECHNIC

LESSON PLAN

Discipline	Semester <u>3rd</u>	Name of the Teaching Faculty
Subject <u>Digital Electronics</u>	No. of days per Week Class Alloted <u>05</u>	Semester from Dt. <u>01-10-2021</u> To Dt. <u>08-01-22</u> No. of Weeks: <u>014</u>
Week	Class Day	Theory / Practical Topics
1st (OCTOBER)	1st Day	Number System - Binary, octal, Decim
	2nd	Conversion from one system to another ^{no. system}
	3rd	Arithmetic Operation - Addition, Subtraction
	4th	Multiplication, Division, 1's & 2's complement
	5th	Digital Code & its application, Binary, excess-3, Gray code.
2nd	0	
3rd	1st	Logic gates:- AND, OR, NOT, NAND
	2nd	Logic gate:- NOR, Exclusive-OR, X-NOR symbol, function, expression, truth table
	3rd	Universal Gates & its Realisation
4th	1st	Boolean algebra, Boolean expressions Demoregan's Theorems.
	2nd	Represent logic Expression: SOP & POS
	3rd	Karnaugh map (3 Variables) forms.
	4th	k-map (4-Variables)
	5th	no minimization of logical expression don't care conditions.
5th (NOVEMBER)	1st	Combinational logic Circuits. Half Adder, Full Adder
	2nd	Half Subtractor, Full Subtractor, Serial & Parallel Binary 4 bit adder.

S. K. Datta
H.O.D. Electronics & Telecomm. Engg
DIP Aithgarh

DHABALESWAR INSTITUTE OF POLYTECHNIC

LESSON PLAN

Discipline	Semester 03	Name of the Teaching Faculty
Subject	No. of days per Week Class Alloted 05	Semester from Dt. 01-10-2021 To Dt. 08-01-22 No. of Weeks: 14
Week	Class Day	Theory / Practical Topics
5th (NOVEMBER)	3rd .	Multiplexer (4:1), Demultiplexer (1:4)
	4th	Decoder, Encoder, Digital comparator
	5th	Seven segment Decoder.
6th	1st	Sequential logic Circuits
	2nd	Principle of flip-flop.
	3rd	SR flip flop using NAND Gate
	4th	Clocked SR flip flop
	5th	Clocked D, JK, T flip flop
7th	1st	Master-Slave flip-flop symbol, logic circuit, truth table.
	2nd	Concept of Racing and how it can be avoided.
	3rd	Registers, Memories & PLD
	4th	Shift Register - Serial-in Serial-out
8th	1st	Serial-in Parallel-out
	2nd	Parallel in Serial out
	3rd	Parallel in Parallel, Universal Shift register



S. K. Pathy
H.O.D. Electronics & Telecommunication

DHABALESWAR INSTITUTE OF POLYTECHNIC LESSON PLAN

Discipline	Semester <u>3rd</u>	Name of the Teaching Faculty
Subject	No. of days per Week Class Alloted <u>05</u>	Semester from Dt. <u>01-08-21</u> To Dt. <u>08-01-22</u> No. of Weeks: <u>014</u>
Week	Class Day	Theory / Practical Topics
8th (NOVEMBER)	4th	Types of Count Counter & application
	5th	Binary Counter, Asynchronous ripple counter.
9th (NOVEMBER)	1st	Decade counter, Ring Counter
	2nd	Concept of memories - RAM, ROM.
(DECEMBER)	3rd	Static RAM, dynamic RAM, PS RAM
	4th	Basic concept of PLD
	5th	Application of PLD
10th (DECEMBER)	1st	Necessity of A/D converter
	2nd	Necessity of D/A converter
	3rd	D/A conversion using weighted resistors method
	4th	R-2R Ladder networks
	5th	weighted resistors network
11th (DECEMBER)	1st	A/D conversion using counter method.
	2nd	A/D conversion using counter method
	3rd	A/D conversion with counter successive approximation

DHABALESWAR INSTITUTE OF POLYTECHNIC LESSON PLAN

Discipline	Semester <u>3rd</u>	Name of the Teaching Faculty
Subject	No. of days per Week Class Alloted <u>05</u>	Semester from Dt. <u>01-08-21</u> To Dt. <u>08-01-22</u> No. of Weeks: <u>14</u>
Week	Class Day	Theory / Practical Topics
11th (DECEMBER)	4th	Various logic families categories to IC fabrication process characteristics of Digital ICs Propagation Delay fan-out, fan-in. Power Dissipation Noise Margin Power Supply requirement Power Supply requirement speed with Reference to logic families speed with Reference to logic families TTL (NAND) Gates, circuit operation & CMOS (NAND), circuit operation CMOS (NOR), circuit operation various applications of TTL & CMOS
	5th	
12th (DECEMBER)	1st	
	2nd	
	3rd	
	4th	
	5th	
13th (DECEMBER)	1st	
	2nd	
	3rd	
	4th	
14th (JANUARY)	1st	
	2nd	
	3rd	
	4th	

[Signature]

[Signature]